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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,291	03/04/2002	Leonel Ernesto Enriquez	50136SE1764TL	6622

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EXAMINER	
BRINEY III, WALTER F	
ART UNIT	**PAPER NUMBER**
2646	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,291	ENRIQUEZ ET AL.	
	Examiner	Art Unit	
	Walter F. Briney III	2646	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takato et al. (US Patent 4,935,960) in view of McAndrews (US Patent 5,160,851).**

Claim 15 is limited to *a circuit arrangement for limiting the DC voltage applied to tip and ring amplifiers of a subscriber line interface circuit (SLIC), each having a first polarity input thereof coupled to a first current flow path to which a DC input voltage is coupled.* Takato discloses a battery feed circuit. See Abstract. Among the many embodiments of Takato is that of figure 38A. This arrangement includes two amplifiers labeled as (10) and (20), where each amplifier drives one of the tip and ring lines of a subscriber loop labeled as A and B. Each amplifier clearly includes two different polarity inputs, where a first polarity input (-) of each amplifier is coupled to a first current flow path to which a DC input voltage V_{BB} is applied; specifically, the current flow path from voltage source V_{BB} into the input of current mirror (2) by way of a resistor. Further note that the current flow path identified is coupled to the first polarity inputs of amplifiers (10). and (20) by way of a chain of current mirrors (3-D), (101) and (102); buffers (94) and (94'); and diode bridges (800) and (800'). With further respect to the claim limitations, Takato depicts in figure 38A that the current mirrors (101) and (102) provide first and

second currents to the second polarity inputs (+) of amplifiers (10) and (20). The current mirror chain of figure 38A clearly illustrates that the currents supplied by the current mirrors (101) and (102) are derived in accordance with the input current flowing from voltage source V_{BB} into the input of current mirror (2) by way of a resistor. Furthermore, the outputs of the current mirrors (101) and (102) are not dependent on feedback current from the outputs of amplifiers (10) and (20). In this way, Takato discloses a first and second current source operative to supply first and second currents to the second polarity input nodes of the tip and ring amplifiers independently of the output of the amplifiers. It is further noted that although amplifiers (10) and (20) do employ feedback, this is not strictly limited by the claim language since the claims merely state that the first and second current sources provide current independent of the amplifier's outputs. Finally, it is submitted that Takato fails to fully anticipate all limitations of the claim because there is no disclosure or suggestion of regulating the DC input voltage V_{BB} in the manner claimed.

McAndrews teaches a rechargeable back-up battery system including a number of battery cells having float voltage exceeding maximum load voltage. See Abstract. In general, the system of McAndrews depicted in figure 1 provides DC power to a general central office load (2). See column 3, lines 52-62. This load corresponds directly to the battery feed circuitry disclosed by Takato. As mentioned in the previous paragraph, Takato does not disclose the origin of supply voltage $-V_{BB}$. It follows that one of ordinary skill in the art would be inherently motivated to combine a prior art teaching of central office power supply. As such, the teachings of McAndrews provide the

necessary supply voltage, and in addition, provide battery backup in the event of loss of AC power, the battery power being regulated to a nominal value by voltage converter (8c) of figure 1. See column 4, lines 15-44, especially lines 39-44.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the rechargeable back-up battery system as taught by McAndrews with the line driving circuitry of Takato because Takato fails to teach how to generate supply voltage $-V_{BB}$ and because the system of McAndrews provides battery backup in the event that AC power is lost.

Claim 16 is limited to *the circuit arrangement according to claim 15*, as covered by Takato in view of McAndrews. As seen in figure 38A of Takato, the outputs of the first and second current sources (101) and (102) are coupled to a combination of resistors (92) and a capacitors (84). As explained in conjunction with figure 11, these elements provide a low pass effect on the outputs of the current sources to remove noise (see column 10, line 52, through column 11, line 5). As the amplifiers (10) and (20) drive the subscriber loop in accordance with the outputs of current sources (101) and (102) whose outputs are noise reduced, it follows that noise is not introduced into the voice paths of amplifiers (10) and (20). Therefore, Takato in view of McAndrews makes obvious all limitations of the claim.

Claim 17 is limited to *the circuit arrangement according to claim 15*, as covered by Takato in view of McAndrews. It is submitted that Takato describes a complete current mirror (2) with respect to figure 11. In particular, an input DC voltage V_{BB} is applied to the combination of a resistor (113) and transistor (112). Figure 11 clearly

depicts that the voltage dividing node (i.e. the node between resistor 113 and transistor 112) is coupled to the current supplies (101) and (102), which supply currents to both the first and second polarity inputs. As shown in the rejection of claim 1, the voltage regulator (8c) of McAndrews is coupled to the tip of the battery (5), and therefore, to the input of the voltage divider, which is coupled to the tip of the battery. Therefore, Takato in view of McAndrews makes obvious all limitations of the claim.

Claim 18 is limited to *the circuit arrangement according to claim 17*, as covered by Takato in view of McAndrews. Figure 11 depicts first and second currents being generated in accordance with the current flowing through the transistor (112) itself. The ends of the transistor (112) defining the voltage dividing node and a reference node. Therefore, Takato in view of McAndrews makes obvious all limitations of the claim.

Claim 19 is limited to *the circuit arrangement according to claim 15*, as covered by Takato in view of McAndrews. It is submitted that Takato describes a complete current mirror (2) with respect to figure 11. In particular, an input DC voltage V_{BB} is applied to the combination of a resistor (113) and transistor (112). Figure 11 clearly depicts that the voltage dividing node (i.e. the node between resistor 113 and transistor 112) is coupled to the current supplies (101) and (102), which supply currents to both the first and second polarity inputs. As shown in the rejection of claim 1, the voltage regulator (8c) of McAndrews is coupled to the tip of the battery (5), and therefore, to the input of the voltage divider, which is coupled to the tip of the battery, and the voltage dividing node by way of resistor (113). Therefore, Takato in view of McAndrews makes obvious all limitations of the claim.

Claim 20 is limited to *the circuit arrangement according to claim 19*, as covered by Takato in view of McAndrews. Figure 11 depicts first and second currents being generated in accordance with the current flowing through the transistor (112) itself. The ends of the transistor (112) defining the voltage dividing node and a reference node. Therefore, Takato in view of McAndrews makes obvious all limitations of the claim.

Response to Arguments

Applicant's arguments filed 24 June 2005 with respect to claims 15-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F. Briney III whose telephone number is 571-272-7513. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFB
10/13/05

SINH TRAN
SUPERVISORY PATENT EXAMINER